REMARKS

By this amendment, claims 1, 17, 26, 28, 48, and 61-63 have been amended. Claims 1-63 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claim 61 has been amended to correct typographical errors, and not for reasons related to patentability.

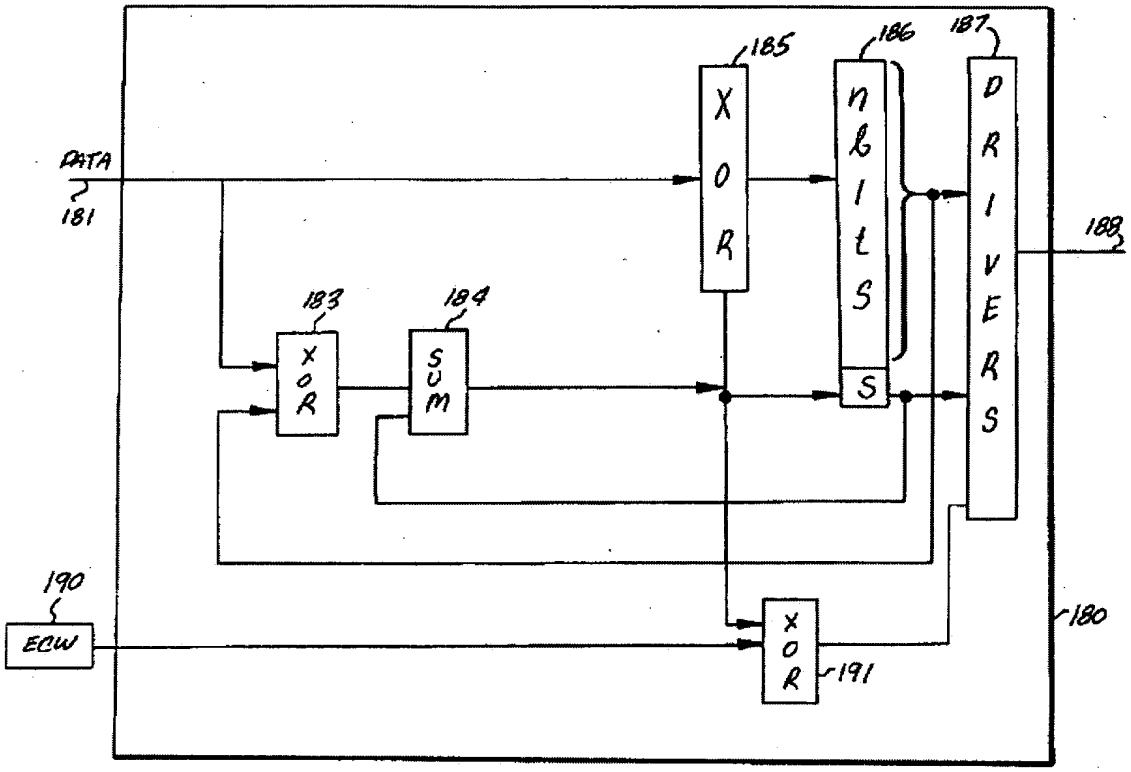
Claim 28 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim has been amended to address the concerns raised in the Office Action. Applicant respectfully requests that the rejection of the claim be withdrawn and the claim allowed.

Claims 1-5, 9-13, 17-18, 21-22, 26-30, 33-36, 43-49, 55-61, and 63 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Curran (US 5,574,921). This rejection is respectfully traversed.

Claim 1 recites, a method of performing bus inversion on first bits to be transmitted on a bidirectional bus comprising, *inter alia*, "capturing a state of previously transmitted bits on the bidirectional bus." Applicant respectfully submits that Curran does not disclose this limitation. To the contrary, Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (which is not labeled in FIG. 6, but presumably runs from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and internal unidirectional input bus 181. Curran FIG. 6 (reproduced below). There is no act of capturing a state of previously transmitted bits on the bidirectional bus as recited

in claim 1. Since Curran does not disclose all the limitations of claim 1, claim 1 and dependent claims 2-5 and 9-13 are not anticipated by Curran.

Curran FIG. 6



Claim 17 recites a method of outputting first bits on a bidirectional bus comprising, *inter alia*, "determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted." Applicant respectfully submits that Curran does not disclose this limitation. To the contrary, Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and internal unidirectional input bus 181. Curran FIG. 6. There is no act of determining from a previous state of the bidirectional bus and a previous state of an

inversion bit associated with the first bits whether the first bits should be inverted as recited in claim 17. Since Curran does not disclose all the limitations of claim 17, claim 17 and dependent claims 18 and 21-22 are not anticipated by Curran.

Claim 26 recites a system comprising, *inter alia*, "a second device connected to said first device by a first bidirectional bus and an associated inversion bit line, said first device transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus" (emphasis added). Applicant respectfully submits that Curran does not disclose this limitation. To the contrary, Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and internal unidirectional input bus 181. There is no act of transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus as recited in claim 26. Since Curran does not disclose all the limitations of claim 26, claim 26 and dependent claims 27-30, 33-36, and 43-47 are not anticipated by Curran.

Claim 48 recites a system comprising, *inter alia*, "a second device connected to the first device by a plurality of bidirectional buses, at least a first bidirectional bus of said plurality of bidirectional buses being associated with a first inversion bit line, said first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted" (emphasis added). Applicant respectfully submits that Curran does not disclose this limitation. To the contrary, Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and

internal unidirectional input bus 181. There is no first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted as recited in claim 48. Since Curran does not disclose all the limitations of claim 48, claim 48 and dependent claims 49 and 55-61 are not anticipated by Curran.

Claim 63 recites a system comprising, *inter alia*, "means for capturing a state of previously transmitted bits on a bidirectional bus." Applicant respectfully submits that Curran does not disclose this limitation. To the contrary, Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and internal unidirectional input bus 181. There is no means for capturing a state of previously transmitted bits on a bidirectional bus as recited in claim 63. Since Curran does not disclose all the limitations of claim 63, claim 63 is not anticipated by Curran.

Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 1-5, 9-13, 17-18, 21-22, 26-30, 33-36, 43-49, 55-61, and 63 be withdrawn and the claims allowed.

Claims 1-5, 9-13, 17-18, 21-22, 26-30, 33-36, 38-39, 41-49, 51-52, 54-61, and 63 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bus-Invert Coding for Low-Power I/O by M.R. Stan and W.P. Burleson (hereinafter "Burleson"). This rejection is respectfully traversed.

Claim 1 recites, a method of performing bus inversion on first bits to be transmitted on a bidirectional bus comprising, *inter alia*, "capturing a state of previously

transmitted bits on the bidirectional bus." Applicant respectfully submits that Burleson does not disclose this limitation. To the contrary, Burleson discloses only that "[a]t the receiver side the contents of the bus must be conditionally inverted according to the *invert* line." Page 54 step 4 (emphasis in original). Applicant respectfully submits that there is no disclosure of capturing a state of previously transmitted bits on the bidirectional bus as recited in claim 1. Since Burleson does not disclose all the limitations of claim 1, claim 1 and dependent claims 2-5 and 9-13 are not anticipated by Burleson.

Claim 17 recites a method of outputting first bits on a bidirectional bus comprising, *inter alia,* "determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted." Applicant respectfully submits that Burleson does not disclose this limitation. To the contrary, Burleson discloses only that "[a]t the receiver side the contents of the bus must be conditionally inverted according to the *invert* line." Page 54 step 4 (emphasis in original). Applicant respectfully submits that there is no disclosure of determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted as recited in claim 17. Since Burleson does not disclose all the limitations of claim 17, claim 17 and dependent claims 18 and 21-22 are not anticipated by Burleson.

Claim 26 recites a system comprising, *inter alia,* "a second device connected to said first device by a first bidirectional bus and an associated inversion bit line, said first device transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus" (emphasis added). Applicant respectfully submits that Burleson does not disclose this limitation. To the contrary, Burleson discloses only that "[a]t the receiver side the contents of the bus must be conditionally inverted according to the *invert* line." Page 54 step 4

(emphasis in original). Applicant respectfully submits that there is no disclosure of transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus as recited in claim 26. Since Burleson does not disclose all the limitations of claim 26, claim 26 and dependent claims 27-30, 33-36, 38-39, and 41-47 are not anticipated by Burleson.

Claim 48 recites a system comprising, *inter alia*, "a second device connected to the first device by a plurality of bidirectional buses, at least a first bidirectional bus of said plurality of bidirectional buses being associated with a first inversion bit line, said first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted" (emphasis added). Applicant respectfully submits that Burleson does not disclose this limitation. To the contrary, Burleson discloses only that "[a]t the receiver side the contents of the bus must be conditionally inverted according to the *invert* line." Page 54 step 4 (emphasis in original). Applicant respectfully submits that there is no disclosure of a first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted as recited in claim 48. Since Burleson does not disclose all the limitations of claim 48, claim 48 and dependent claims 49, 51-52, and 54-61 are not anticipated by Burleson.

Claim 63 recites a system comprising, *inter alia*, "means for capturing a state of previously transmitted bits on a bidirectional bus." Applicant respectfully submits that Burleson does not disclose this limitation for at least the reasons set forth above. Since Burleson does not disclose all the limitations of claim 63, claim 63 is not anticipated by Burleson.

Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 1-5, 9-13, 17-18, 21-22, 26-30, 33-36, 38-39, 41-49, 51-52, 54-61, and 63 be withdrawn and the claims allowed.

Claims 1, 13-15, 17, 22-24, 26, 36-37, 48, 50, and 63 stand rejected under 35 U.S.C. § 102(b) as being anticipated by de la Iglesia (US 6,490,703). This rejection is respectfully traversed.

Claim 1 recites, a method of performing bus inversion on first bits to be transmitted on a bidirectional bus comprising, *inter alia*, "capturing a state of previously transmitted bits on the bidirectional bus." Applicant respectfully submits that de la Iglesia does not disclose this limitation. To the contrary, de la Iglesia discloses that the "determination to flip in selective bus inversion is made by comparing the number of logic state bits of the present data to the total number of bits in the present data. If more than half of the bits are logic one, the entire data string may be flipped." Col. 5, ln. 6-10 (emphasis added). Applicant respectfully submits that there is no disclosure of capturing a state of previously transmitted bits on the bidirectional bus as recited in claim 1. Since de la Iglesia does not disclose all the limitations of claim 1, claim 1 and dependent claims 13-15 are not anticipated by de la Iglesia.

Claim 17 recites a method of outputting first bits on a bidirectional bus comprising, *inter alia*, "determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted." Applicant respectfully submits that de la Iglesia does not disclose this limitation. To the contrary, de la Iglesia discloses that the "determination to flip in selective bus inversion is made by comparing the number of logic state bits of the present data to the total number of bits in the present data. If more than half of the bits are logic one, the entire data string may be flipped." Col. 5, ln. 6-10 (emphasis added).

Applicant respectfully submits that there is no disclosure of determining from a previous state of the bidirectional bus and a previous state of an inversion bit associated with the first bits whether the first bits should be inverted as recited in claim 17. Since de la Iglesia does not disclose all the limitations of claim 17, claim 17 and dependent claims 22-26 are not anticipated by de la Iglesia.

Claim 26 recites a system comprising, *inter alia*, "a second device connected to said first device by a first bidirectional bus and an associated inversion bit line, said first device transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus" (emphasis added). Applicant respectfully submits that de la Iglesia does not disclose this limitation. To the contrary, de la Iglesia discloses that the "determination to flip in selective bus inversion is made by comparing the number of logic state bits of the present data to the total number of bits in the present data. If more than half of the bits are logic one, the entire data string may be flipped." Col. 5, ln. 6-10 (emphasis added). Applicant respectfully submits that there is no disclosure of transmitting first bits over the first bidirectional bus to the second device by capturing a state of previously transmitted bits on the first bidirectional bus as recited in claim 26. Since de la Iglesia does not disclose all the limitations of claim 26, claim 26 and dependent claims 36-37 are not anticipated by de la Iglesia.

Claim 48 recites a system comprising, *inter alia*, "a second device connected to the first device by a plurality of bidirectional buses, at least a first bidirectional bus of said plurality of bidirectional buses being associated with a first inversion bit line, said first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted" (emphasis added). Applicant respectfully submits that de la Iglesia does not disclose this limitation. To

the contrary, de la Iglesia discloses that the "determination to flip in selective bus inversion is made by comparing the number of logic state bits of the present data to the total number of bits in the present data. If more than half of the bits are logic one, the entire data string may be flipped." Col. 5, ln. 6-10 (emphasis added). Applicant respectfully submits that there is no disclosure of a first device transmitting first bits over the first bidirectional bus by determining from a previous state of the first bidirectional bus and a previous state of an inversion bit on the first inversion bit line whether the first bits should be inverted as recited in claim 48. Since de la Iglesia does not disclose all the limitations of claim 48, claim 48 and dependent claim 50 are not anticipated by de la Iglesia.

Claim 63 recites a system comprising, *inter alia*, "means for capturing a state of previously transmitted bits on a bidirectional bus." Applicant respectfully submits that de la Iglesia does not disclose this limitation for at least the reasons set forth above. Since de la Iglesia does not disclose all the limitations of claim 63, claim 63 is not anticipated by de la Iglesia.

Applicant respectfully requests that the 35 U.S.C. § 102(b) rejection of claims 1, 13-15, 17, 22-24, 26, 36-37, 48, 50, and 63 be withdrawn and the claims allowed.

Claims 6-8, 19-20, 31-32, 38-42, 51-54, and 62 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curran. This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Applicant respectfully submits that even when considered in combination with the assertions in the Office Action, Curran does not teach or suggest all limitations of independent claim 62.

Claim 62 recites a system comprising, *inter alia*, "first, second, and third devices connected to each other by a first bidirectional bus and an associated inversion bit line, said first device transmitting first bits over the first bidirectional bus to one of the second and third device by capturing a state of previously transmitted bits on the first bidirectional bus, capturing a state of an inversion bit on the inversion bit line and determining from the captured state of the previously transmitted bits whether the first bits should be inverted" (emphasis added). Curran does not teach or suggest this limitation. To the contrary, Curran teaches Curran discloses only an internal unidirectional input bus 181 and XOR circuit 183, which receives data only from the internal feedback bus 182 (from the output of the nbit portion of register 186 to the lower input of XOR circuit 183) and internal unidirectional input bus 181. Curran FIG. 6. There is no transmitting first bits over the first bidirectional bus to one of the second and third device by capturing a state of previously transmitted bits on the first bidirectional bus as recited in claim 62. Thus, the assertions in the Office Action do not remedy the deficiency of Curran. Since Curran does not teach or suggest all of the limitations of claim 62, claim 62 is not obvious over the cited reference.

Claims 6-8, 19-20, 31-32, 38-42, and 51-54 depend, respectively, directly, or indirectly from independent claims 1, 17, 26, and 48, and are allowable for at least the reasons set forth above and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 6-8, 19-20, 31-32, 38-42, 51-54, and 62 be withdrawn and the claims allowed.

Claims 6-8, 19-20, 31-32, 40, 53, and 62 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Burleson. This rejection is respectfully traversed. Even when considered in combination with the assertions in the Office Action, Burleson does not teach or suggest all limitations of independent claim 62.

Claim 62 recites a system comprising, *inter alia*, "first, second, and third devices connected to each other by a first bidirectional bus and an associated inversion bit line, said first device transmitting first bits over the first bidirectional bus to one of the second and third device by capturing a state of previously transmitted bits on the first bidirectional bus, capturing a state of an inversion bit on the inversion bit line and determining from the captured state of the previously transmitted bits whether the first bits should be inverted" (emphasis added). Burleson does not teach or suggest this limitation. To the contrary, Burleson discloses only that "[a]t the receiver side the contents of the bus must be conditionally inverted according to the *invert* line." Page 54 step 4 (emphasis in original). Applicant respectfully submits that there is no disclosure of transmitting first bits over the first bidirectional bus to one of the second and third device by capturing a state of previously transmitted bits on the first bidirectional bus as recited in claim 62. Thus, the assertions in the Office Action do not remedy the deficiency of Burleson. Since Burleson does not teach or suggest all of the limitations of claim 62, claim 62 is not obvious over the cited reference.

Claims 6-8, 19-20, 31-32, 40, and 53 depend, respectively, from independent claims 1, 17, 26, and 48, and are allowable for at least the reasons set forth above and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 6-8, 19-20, 31-32, 40, 53, and 62 be withdrawn and the claims allowed.

Claims 16 and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over de la Iglesia. This rejection is respectfully traversed. Claims 16 and 25 depend, respectively, from independent claims 1 and 17, and are allowable for at least the reasons set forth above and on their own merits. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 16 and 25 be withdrawn and the claims allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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